1.A method of fabricating a high quantum efficiency photodiode comprising:

forming a well region of a first conductivity in a substrate of a second conductivity opposite to said first conductivity wherein said well region in said substrate forms said photodiode;

forming an isolation region within said substrate overlying said well region;

removing a portion of said isolation region overlying said well region;

thereafter depositing a stop layer on said well region; and

depositing an interlevel dielectric layer overlying said stop layer to complete fabrication of said high performance photodiode.

2.The method according to Claim 1 wherein said well region is an N-well and said substrate is a P-substrate.

3. The method according to Claim 1 wherein said well region is a P-well and said substrate is an N-substrate.

4. The method according to Claim 1 wherein said isolation region is a shallow trench isolation.

5. The method according to Claim 1 wherein said stop layer comprises silicon nitride or silicon oxynitride.

6.The method according to Claim 1 wherein said stop layer has a thickness of between about 400 and 1000 Angstroms.

7. The method according to Claim 1 wherein said interlevel dielectric layer comprises silicon oxide.

8. The method according to Claim 1 where said interlevel dielectric layer has a thickness of between about 7000 and 13,000 Angstroms.

9. The method according to Claim 1 wherein a refraction index of said stop layer is less than a refraction index of said well region and greater than a refraction index of said interlevel dielectric layer.

10. The method according to Claim 1 wherein said step of depositing a stop layer comprises forming a stop layer for a CMOS borderless contact process.

11. A method of fabricating a high quantum efficiency photodiode comprising:

forming a well region of a first conductivity in a substrate of a second conductivity opposite to said first conductivity wherein said well region in said substrate forms said photodiode;

forming an isolation region within said substrate overlying said well region;

fabricating semiconductor device structures in a CMOS process;

removing a portion of said isolation region overlying said photodiode;

thereafter depositing a stop layer directly on said well region; and

depositing an interlevel dielectric layer overlying said stop layer to complete fabrication of said high performance photodiode.

12.The method according to Claim 11 wherein said well region is an N-well and said substrate is a P-substrate.

13. The method according to Claim 11 wherein said well region is a P-well and said substrate is an N-substrate.

14. The method according to Claim 11 wherein said isolation region is a shallow trench isolation.

15. The method according to Claim 11 wherein said semiconductor device structures comprise gate electrodes and source and drain regions formed in and on said substrate in areas away from said photodiode.

16. The method according to Claim 11 wherein said stop layer comprises silicon nitride or silicon oxynitride.

17.The method according to Claim 11 wherein said stop layer has a thickness of between about 400 and 1000 Angstroms.

18. The method according to Claim 11 wherein said interlevel dielectric layer comprises silicon oxide.

19. The method according to Claim 11 where said interlevel dielectric layer has a thickness of between about 7000 and 13,000 Angstroms.

20. The method according to Claim 11 wherein a refraction index of said stop layer is less than a refraction index of said well region and greater than a refraction index of said interlevel dielectric layer.

21. The method according to Claim 11 wherein said step of depositing a stop layer comprises forming a stop layer for a CMOS borderless contact process.

22.A high quantum efficiency image sensor comprising:

a well region of a first conductivity in a substrate of a second conductivity opposite to said first conductivity wherein said well region in said substrate forms a photodiode;

an isolation region within said substrate overlying edge portions of said photodiode;

a stop layer overlying said photodiode; and

an interlevel dielectric layer overlying said stop layer.

23.The image sensor according to Claim 22 wherein said well region is an N-well and said substrate is a P-substrate.

24. The image sensor according to Claim 22 wherein said well region is a P-well and said substrate is an N-substrate.

25. The image sensor according to Claim 22 wherein said isolation region is a shallow trench isolation.

26. The image sensor according to Claim 22 wherein said stop layer comprises silicon nitride or silicon oxynitride.

27. The image sensor according to Claim 22 wherein said stop layer has a thickness of between about 400 and 1000 Angstroms.

28. The image sensor according to Claim 22 wherein said interlevel dielectric layer comprises silicon oxide.

29. The image sensor according to Claim 22 where said interlevel dielectric layer has a thickness of between about 7000 and 13,000 Angstroms.

30. The image sensor according to Claim 22 wherein a refraction index of said stop layer is less than a refraction index of said well region and greater than a refraction index of said interlevel dielectric layer.